83256 #6/A PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re U.S. Patent Application)
)
Applicant: Infineon Technologies)
)
Serial No.: Not Yet Assigned)
)
Filed: Herewith)
)
For: **ELECTRONIC PHASE-LOCKED LOOP**)
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)

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This is a Preliminary Amendment for entry in the above-identified application.

In the Claims:

Please amend the claims as follows:

1. (amended) An electronic phase-locked loop for jitter-attenuated clock multiplication, in particular as part of an integrated circuit for integrated services communications networks, data communication or networks in which the frequency of a controllable oscillator is set in such a way that it corresponds to a reference frequency, the output signal of the oscillator being compared with the reference frequency in a digital phase detector, and the output signal of the digital phase detector setting the frequency of the oscillator via a digital regulated system, wherein the digital phase-locked loop is connected up to an additional analog phase detector and a lock detection for activation.